

ABSTRACT OF THE DISCLOSURE

A memory controller can accurately synchronize a strobe signal generated from a clock signal with respect to digital data for inputting/outputting digital data to/from a semiconductor memory device, such as double-data-rate (DDR) synchronous dynamic random access memory (SDRAM), or the like. Output holding circuits (108) can be situated adjacent to corresponding data output terminal (105). One of $(n/2)$ output delay circuits (112) can be situated adjacent to every two of n signal output terminals (112). Wiring lengths from output holding circuits (108) to data output terminals (105) can be made essentially equal to wiring lengths between the output of each delay circuit (112) and the corresponding signal output terminals (112). A delay of digital data transmitted from output holding circuits (108) to data output terminals (105) can be made essentially equal to a delay of an output strobe signal transmitted from output delay circuits (112) to corresponding signal output terminals (106).